REMARKS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 1, 2, 5-9 and 11-22 are pending. Claims 15-21 are withdrawn. Claims 3, 4 and 10 have been canceled. Claims 1, 6, 12, 15 and 19 are independent. Claims 1, 6, 12 and 13 are amended. Reconsideration of this application, as amended, is respectfully requested.

Claim Objections

Claims 4 and 7 are objected to because of informalities. It is respectfully submitted that claims 1 and 6 are amended to provide antecedent basis for the recitation in dependent claims 4 and 7. Therefore, it is respectfully requested that the objection to claims 4 and 7 be withdrawn.

Claim Rejections under 35 U.S.C. § 102/103

Claims 1, 2, 4 and 5 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,414,730 to Akamatsu et al. Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Akamatsu et al. in view of U.S. Patent No. 5,926,235 to Han et al. Claims 6-9 and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,091,466 to Kim et al. in view of Lyu. Claims 6 and 10-14 are rejected under 35 U.S.C. § 102(e) as being anticipated by Kim et al. These rejections are respectfully traversed.

While not conceding the appropriateness of any of the rejections, but merely to expedite the prosecution of the instant application, independent claim 1 is amended to recite a combination of elements in an array substrate for a liquid crystal display device, including "a storage capacitor including a portion of the gate line as a first storage electrode, a portion of the gate insulation layer, and a second storage electrode having an island shape, wherein the first storage electrode is formed of the same material as the gate electrode and the second storage electrode is formed of the same material as the source and drain electrodes and disposed on the gate insulation layer."

Independent claims 6 and 12 are amended to recite combinations of elements in an array substrate, including "a gate insulation film formed over the gate line, wherein a portion of the pixel electrode is formed directly on the gate insulation film in a whole of a pixel region defined by the gate and data lines."

It is respectfully submitted that the combinations of elements set forth in independent claims 1, 6 and 12 are not anticipated or made obvious by the cited art of record, including Akamatsu et al., Han et al., Kim et al. or Lyu.

Akamatsu et al. discloses a liquid crystal display device which includes a substrate 51, a gate insulation film 53 and an interlayer insulation film 68 and a pixel electrode 69 as shown in Fig. 7A. The pixel electrode 69 is formed on the interlayer insulation film 68 and a portion of a semiconductor layer 54. However, Akamatsu et al. does not teach or suggest "a storage capacitor including a portion

of the gate line as a first storage electrode, a portion of the gate insulation layer, and a second storage electrode having an island shape, wherein the first storage electrode is formed of the same material as the gate electrode and the second storage electrode is formed of the same material as the source and drain electrodes and disposed on the gate insulation layer," as recited in claim 1, as amended.

In rejecting claim 4, which has now been incorporated into claim 1, the Office Action relies on Han for a teaching of an array substrate with a thin film transistor and a storage capacitor. However, Han does not teach or suggest that "the second storage electrode is formed of the same material as the source and drain electrodes and disposed on the gate insulation layer", and therefore fails to cure the deficiencies of Akamatsu et al.

Kim et al. discloses a liquid crystal display including a substrate 101, a gate insulation layer 117, a drain electrode 131, a semiconductor layer 133, a source electrode 121, a passivation layer 137, and a pixel electrode 141 as shown in Fig. 5F. The pixel electrode 141 is formed mainly on the passivation layer 137 and touches portions of gate electrode 111 and a drain electrode 131. In Kim, the contact hole penetrates the drain electrode 131 and exposes the dummy drain electrode 139. This feature is different from the present invention where the passivation layer pattern exposes a portion of a side surface of the drain electrode.

In addition, Kim et al. does not teach or suggest "a gate insulation film formed over the gate line, wherein a portion of the pixel electrode is formed directly on the gate insulation film in a whole of a pixel region defined by the gate and data lines," as recited in claims 6 and 12, as amended.

The Office Action relies on Lyu for a teaching of a semiconductor layer and an ohmic contact layer having ends lined with and directly below corresponding ends of the source electrode and drain electrode. However, Lyu does not teach or suggest the above cited limitations of claims 6 and 12, and therefore fail to cure the deficiencies of Kim et al.

For at least the foregoing reasons, independent claims 1, 6 and 12 and their dependent claims (due to their dependencies) are patentable over the applied prior art and reconsideration and withdrawal of the rejections based on these reasons are respectfully requested.

CONCLUSION

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Sam Bhattacharya (Reg. No. 48,107) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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